We claim:

1. A digital intermediate frequency QAM modulator using parallel processing, comprising:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data;

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations;

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of

said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data.

2. A digital intermediate frequency QAM modulator using parallel processing, comprising:

a serial-to-parallel data converter operatively connected to receive serial data, wherein said serial-to-parallel data converter converts a string of serial data to a plurality of parallel data;

an I and Q mapper operatively connected to receive said plurality of parallel data and determine its I and Q locations;

a plurality of look-up-tables (LUTs) operatively connected to receive and store said I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN};

at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data.

3. The digital intermediate frequency QAM modulator using parallel processing of claim 2, wherein said at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1

to IQ_{IQN} comprises nx2 multiplexers, where n is an integer, and wherein at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers.

4. A digital intermediate frequency QAM modulator using parallel processing, comprising:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN};

a first multiplexer operatively connected to collect from said plurality of registers only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

a second multiplexer operatively connected to collect from said plurality of registers only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said odd subscript data and said even subscript data to analog data.

5. The digital intermediate frequency QAM modulator using parallel processing of claim 4, wherein said at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers, where n is an integer, and wherein at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers.

6. A digital intermediate frequency QAM modulator using parallel processing, comprising:

a plurality of look-up-tables (LUTs) operatively connected to receive and store I and Q locations, wherein the I LUTs are configured I_1 to I_N, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

a plurality of adders operatively connected to receive and add said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

a plurality of registers operatively connected to collect and store said output data comprising IQ_1 to IQ_{IQN}; and

a digital to analog converter operatively connected to convert said output data comprising IQ_1 to IQ_{IQN} to analog data.

7. A method for processing data with a digital intermediate frequency QAM modulator using parallel processing, comprising:

receiving and converting a string of serial data into a plurality of parallel data;

determining the I and Q locations of said plurality of parallel data;

storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_N, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing said output data comprising IQ_1 to IQ_{IQN} in a plurality of registers; and

converting said output data comprising IQ_1 to IQ_{IQN} to analog data in a digital to analog converter.

8. A method for processing data in a digital intermediate frequency QAM modulator using parallel processing, comprising:

receiving and converting a string of serial data to a plurality of parallel data;

receiving said plurality of parallel data in an I and Q mapper and determine the I and Q locations of said plurality of parallel data;

receiving and storing said I and Q locations in a plurality of look-up-tables (LUTs), wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding said I and Q locations stored within said plurality of LUTs in a plurality of adders, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN};

collecting, in a multiplexer, from said plurality of registers, the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

collecting, in a multiplexer, from said plurality of registers, the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

converting, a digital to analog converter, said odd subscript data and said even subscript data to analog data.

9. The method of claim 8, wherein said at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers, where n is an integer, and wherein at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers.

10. A method, comprising:

receiving and storing in a plurality of look-up-tables (LUTs), I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN};

collecting in a first multiplexer only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN};

collecting in a second multiplexer only even subscript output data from said output data comprising IQ_1 to IQ_{IQN}; and

converting in a digital to analog converter said odd subscript data and said even subscript data to analog data.

11. The method of claim 10, wherein said at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only odd subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers, where n is an integer, and wherein at least one multiplexer operatively connected to collect from said plurality of registers the subscript output data comprising only even subscript output data from said output data comprising IQ_1 to IQ_{IQN} comprises nx2 multiplexers.

12. A method for processing data with a digital intermediate frequency QAM modulator using parallel processing, comprising:

receiving and storing, in a plurality of look-up-tables (LUTs) I and Q locations, wherein the I LUTs are configured I_1 to I_n, wherein N is the highest number of I LUTs of said plurality of LUTs, wherein the Q LUTs are configured Q_1 to Q_X, wherein X is the highest number of Q LUTs of said plurality of LUTs;

receiving and adding in a plurality of adders said I and Q locations stored within said plurality of LUTs, wherein said plurality of adders are configured A_1 to A_{AN}, wherein AN is the highest number of adders of said plurality of adders, wherein each I and Q having a particular subscript are added in the adder having the same subscript to produce output data comprising IQ_1 to IQ_{IQN};

collecting and storing in a plurality of registers said output data comprising IQ_1 to IQ_{IQN}; and

converting in a digital to analog converter said output data comprising IQ_1 to IQ_{IQN} to analog data.